Remarks

New Matter Objections To The Specification:

The Law of New Matter & The Claims and Description Requirement:

When an amendment changes the scope of a claim in such a way as to justify an assertion that it is directed to a different invention than was the original claim, it is proper to inquire whether the newly claimed subject matter was described as the invention of the applicant in the patent application when filed. Harmon, *Patents and the Federal Circuit*, (4th ed. 1998), Section 5.5, p. 196 (hereafter Harmon).

If the essence of the original disclosure supports the new claim limitation or addition to the specification, it is not new matter. In re Wright, 866 F. 422, 9 USPQ2nd. 1649 (Fed. Circuit 1989).

The adequate written description requirement, which is distinct from best mode and enablement, serves to ensure that the inventor had possession, as of the filing date of the application, of the specific subject matter claimed by him. How the specification accomplishes this is not important. The applicant does not have to use any particular form of disclosure, and the fact that the disclosure is very short is immaterial. Harmon, Section 5.5. Under proper circumstances, drawings alone may provide a description of an invention which is adequate to satisfy the written description requirement of 35 USC section 112. Harmon, Section 5.5, p. 197. **An ipsis verbis disclosure is not necessary to satisfy the written description requirement.**

The new matter issue is judged from the standpoint of one of ordinary skill in the art. Harmon, section 5.5, p. 195. If one skilled in the art, reading the original specification, would immediately discern the limitation at issue in the parent application, then it is not new matter. In other words, the question is, does the original disclosure being relied upon for support reasonably convey to the artisan that the invention had

possession of the invention in the later claimed subject matter. In other words the question on support for a new limitation in a claim is not one of literal ipsis verbis support, but does the specification, as originally filed, reasonably convey to one skilled in the art that the invention had possession of the claimed Whether invention at the time of the original filing date. Harmon, Section 5.5, p. 197. particular technical information is new matter depends upon the nature of the disclosure, the state of the art, and the nature of the added matter.

The initial burden to make out a prima facie case is on the Examiner. If the specification contains a description of the claimed invention albeit not in the identical words used, then the Examiner must provide reasons why one of ordinary skill in the art would not consider the disclosure sufficient. Harmon, section 5.5, p. 198.

A function or property which in inherent in a claimed product can be expressly described in an amendment and is not new matter. Harmon, section 5.5, p. 202.

Analysis of New Matter Rejections On A Line-By-Line Basis.

Without admitting that any of the changes were new matter, but in an effort to speed the prosecution of this case to issuance, most of the additions to the substitute specification previously filed were cancelled. The undersigned however insists that the remaining additions previously made and not cancelled here are not new matter because the original specification and drawings included the subject matter either in the table/appendix or in the original drawings. The undersigned also makes one amendment regarding the floating gate description in the specification to conform that part of the specification to what was clearly disclosed in the original drawings and to conform the language to what the Board found to be the meaning of self aligned with respect to the floating gate. All page and line references are to the substitution specification.

The Examiner objected to the addition "wells 62 and 64" at page 8, line 11 and "and 64" on line 5 of Table 1 at page 15 of the substitute specification. Neither change is new matter because the original Figures 8b and 8c show two N-Wells 62 and 64 being formed, and original line 4 of Table 1 at page 15 teaches preparing to implant the two N Wells 62 and 64 using a "twin well mask". One skilled in the art would clearly realize that the two changes the Examiner said were new matter actually only conformed page 8, line 11 and line 5 of Table 1 to the original drawing and original line 4 of Table 1.

The Examiner rejected the "300 angstroms thick grown oxide layer" addition at page 8, line 24. In response, the "300 angstroms thick" and "is grown" language added to the previous substitute specification has been cancelled. The oxide layer part is not new matter because original Figures 8A, and 8B & 8C showed an oxide/nitride layer 68. Therefore this part of the addition is not new matter since it only conforms the specification to the original drawings.

The Examiner objected to the "vertically down" and "vertical" additions to page 10, line 10. In response, these additions have been cancelled since Figure 15B clearly shows the result of the anisotropic etch as wells formed vertically down into the subsratate such that the axis of the well is orthogonal to the surface of the substrate.

The Examiner objected to the change from "recessed gate windows" to "wells" at page 10, line 20. In response, this change has been cancelled and the original language restored. Similar changes at page 10, line 17 and page 11, lines 1& 2 have been cancelled.

The Examiner objected to the addition of "the entire horizontal top surface of the substrate extending laterally in all directions", at page 10, line 21. In response, this

change has been modified to "and covers the top surface of the substrate". This addition is not new matter because the original drawings at Figures 16A, 16B and 16C show the nitride layer 92 covering the top surface of the substrate.

The Examiner objected to the change at page 10, line 23 and 24 of the substitute specification markup. In response, this change has been cancelled.

The Examiner objected to the sentence starting "Next, a layer of oxide insulator... ." starting at page 10, line 27 extending to page 11, line 1. In response, the sentence has been changed to simply read, "Next, a layer of oxide insulator 96 is grown on the bottoms of the recessed gate windows 88 and 90". This addition is not new matter, because this subject matter was disclosed in the original Appendix (now labeled Table 1) at line 29 on page 17. So the change merely conforms one part of the specification to another. Growth of oxide layer 96 on the bottoms of the recessed gate windows is also disclosed in original Figure 18B.

The Examiner objected to the addition at page 11, line 3 and 4 of "from the vertical walls of the wells 88 and 90". In response, this change has been cancelled.

The Examiner objected to the addition at page 11, lines 6-7. In response, this addition has been modified to "on the walls of the recessed gate windows 88 and 90". This addition is not new matter because original Figure 20B shows a gate oxide layer 100 on the walls of the recessed gate windows 88 and 90. This addition is also supported by line 32 of Table 1 which states that a thin gate oxide layer 100 having a thickness of from 90 to 100 angstroms is grown. Original Figure 20B shows that this gate oxide layer is grown on the walls of the recessed gate windows 88 and 90.

The Examiner also objected to all the changes to Table 1. In response to this rejection, most of the changes to Table 1 have been cancelled. The change to Line 54 of the table is only to renumber the line number from 53 to 54 because the original appendix table had two line 53. Inspection will show that the text of Table 1, Line 54 is identical to the original text of the second line 53 of the original appendix. Further, in partial response to this objection, the addition to line 32 of Table 1 has been deleted although this language only states the inherent function of this gate oxide layer 100.

The Examiner objected to the changes at page 11, line 8. In response to this objection the proposed changes have been cancelled.

The Examiner objected to the change at page 11, lines 17-19*. In response, this change has been amended as follows. To integrate the teachings of original Table 1, steps 33 and 34 and the original Figure 21B into this portion of the specification which describes the process for making the floating gate, the following amendment was made to the passage starting at page 11, line 16 of the substitute specification markup enclosed herewith. The bold text is text that I have added by this amendment to clarify the structure of the floating gate 102 and the process for making it:

> To form the floating gate, the doped polysilicon is etched back off all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure shown in Figure 5 <u>and are self aligned with the walls of the **recessed gate windows** wells 88 and 90 **because no horizontal component of doped polysilicon is left on the surface of the substrate or on the bottom of the recessed gate windows which means no portion of the doped polysilicon will ever extend beyond the perimeter of the recessed gate window (see Figure 21B for the configuration of the doped polysilicon floating gate 102 after the etchback). No mask is used for the etchback of the doped polysilicon layer 102 as can be seen from study of Table 1 steps 33 and 34 where no mask is recited as being used during the etchback. All steps that use masks are recited in Table 1 as using a mask and the mask number is given in the third**</u>

> **column from the left.** <u>The floating gates can be made without using a mask because of the fact that the etchback removes all portions of polysilicon 102 on horizontal surfaces on top of the substrate and at the bottoms of the wells 88 and 90</u>.

The language is bold is not new matter because it only states what the Board recognized as teachings that are present in this specification. Specifically, these changes state what is taught in original steps 33 and 34 of Table 1 (that an etchback is used to etch all doped polysilicon off all horizontal surfaces and that no mask is used for either step 33 nor step 34). **These changes also state what the Board recognized as being taught in the original specification that the floating gate is self aligned because it has no horizontal component on the surface of the substrate nor on the bottom of the well and therefore no doped polysilicon of the floating gate will extend beyond the perimeter of the trench.**

Further, this change is not new matter because it only states in words what original Figure 21B shows. One skilled in the art would clearly know that the floating gate was self aligned because the original specification language at page 11, lines 14-17 teaches:

> "To form the floating gate the doped polysilicon is etched back off all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure of Figure 5".

Original Figure 21B clearly shows that the doped polysilicon 102 has been removed from the horizontal surface above the recessed gate windows 88 and 90. It also shows the doped polysilicon has been removed from the horizontal bottoms of the recessed gate windows 88 and 90 and that the doped polysilicon has been removed from the uppermost parts of the vertical walls of the recessed gate windows. This was taught in the original

specification portion quoted above as having been done with an etch and no mention of a mask or photoresist is made. See also Table 1, steps 33 and 34 of the original specification which teach depositing doped polysilicon layer 102 and then etching it back off all horizontal surfaces and which recites no mask being used when these steps are done. Note that all other steps in Table 1 which use masks have masks and the mask numbers recited in the third column from the left in Table 1. **One skilled in the art knows from the original teachings of the specification at page 11, from Table 1 steps 33 and 34 and from Figure 21B that the process described of using an etch without a mask to remove doped polysilicon from only the horizontal surfaces creates self aligned floating gates. The Board of Appeals recognized this in its 26 September 2001 opinion by stating that a self aligned floating gate "will not have any horizontal component on the surface of the substrate or on the bottom of the well and therefore will not extend beyond the perimeter of the trench."** These floating gates are only on the vertical walls of the recessed gate windows and do not extend up over the top edges of the walls of the recessed gate windows and out onto the surrounding horizontal surfaces. That is why they are self-aligned. There is no mask used so there is never a registration error which would cause some horizontal component on the surface of the substrate or on the bottom of the wells. That means the doped polysilicon will never extend up over the top edges of the wells onto the surrounding horizontal surfaces nor will there ever be a horizontal component of doped polysilicon on the bottoms of the wells. That means that the EEPROM cells can be made much smaller because there is no need to have the larger design rule clearances around the wells that would be necessary if the floating gates were made using a mask.

Changes made to an application that are necessarily supported by the information disclosed in the specification are not considered new matter under 35 USC 132. The CCPA has stated the following general rule for determining when subject matter is inherently disclosed in the specification:

> By disclosing in a patent application a device that inherently performs a function, operates according to a theory, or has an advantage, a patent applicant necessarily discloses that function, theory or advantage even though he says nothing concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.

In re Smythe, 480 F.2d 1376, 178 USPQ 279, 285 (CCPA 1973).

Consider also the rule that drawings may provide an adequate written description of the invention in the event the written disclosure portion of the application inadvertently omitted such a written description. The CCPA described the general test for determining whether a drawing can constitute an adequate written description of the invention under Section 112, first paragraph:

> The practical, legitimate inquiry in each case of this kind is what the drawing in fact discloses to one skilled in the art. Whatever it does disclose may be added to the specification in words without violation of the statute and rule which prohibits "new matter," 35 U.S.C. 132, Rule 118, for the simple reason *that* what *is* originally disclosed cannot be "new matter" within the meaning of this law. If the drawing, then, contains the necessary disclosure, it *can* "form the basis of a valid claim."

In re Wolfensperger, 302 F.2d 950, 133 USPQ 537 (CCPA 1962).

Here, the original Table 1, steps 33 and 34 taught making the floating gate without using a mask and using an etchback process which only removed doped polysilicon layer 102 from horizontal surfaces. Figure 21B originally showed and still shows that the completed structure after the etchback does not have any horizontal component of doped polysilicon layer 102 on the horizontal surfaces of the substrate or

the bottom of the well. This original disclosure of the process to make the floating gate inherently disclosed a self aligned floating gate that is made without using a mask and which has the characteristic that no doped polysilicon will be on the top surface of the substrate nor on the bottom of the well and therefore will never extend beyond the perimeter of the recessed gate window or well. That is what the Board recognized. That is also what a self aligned floating gate is, and that is the way the Board defined the self aligned floating gate in this way in its opinion. The claims have all been amended herein to define the self aligned floating gate in this way. To amend the specification to add a description of what is inherently disclosed in original Table 1, steps 33 and 34 and original Figure 21B is not new matter.

The Examiner objected to the addition at page 12, lines 11-12. In response, this addition has been cancelled.

The Examiner objected to the addition at page 12, line 14. In response, this addition has been cancelled.

The Examiner objected to the addition at page 13, line 8. In response, this addition has been cancelled.

The Examiner objected to the addition at page 13, line 19. In response, this addition has been cancelled.

The Examiner objected to the addition at page 14, lines 8-9. In response, this addition has been cancelled.

The Examiner objected to the addition at page 14, lines 12-16. In response, this addition has been cancelled.

CHANGES TO TABLE 1

The Examiner has objected wholesale to all changes to Table 1 starting at page 15. In response most of these changes have been cancelled, but some have been retained because they clearly are not new matter as having been disclosed in the original specification or drawings. The specific places in the specification or drawings where changes which have been retained were originally disclosed are detailed below.

The changes to lines 1, 5, 6, and 7 have not been cancelled because they make the table more clear and are not new matter. Specifically, original line 4 indicates a twin well mask is used to form a layer of photoresist, and original Figures 7B and 7C show that two N-type wells 62 and 64 are formed. Therefore the changes to lines 5, 6 and 7 do not add new subject matter.

The change to line 20 of Table 1 has not been cancelled because it is not new matter. This change only conforms line 20 of the Table 1 to the original specification teachings at page 9, lines 15-20. This portion of the specification coupled with original Figures 12A, 12B and 12C teach removing the nitride portion of the ONO layer over the EEPROM active area to leave a layer of pad oxide over the EEPROM area.

The change to line 21 of Table 1 has been cancelled.

The change to line 22 of Table 1 has been cancelled.

The changes to lines 25 and 26 of Table 1 have been cancelled.

The change to line 28 has been cancelled in part but the "anisotropic" addition has not been cancelled. This addition is not new matter because it merely conforms line 28 of the Table to the original teachings of the specification at page 10, line 23 of the substitute specification.

The changes to lines 29 and 32 of the table have been cancelled.

The change to line 30 of the table has been revised to conform it to the exact teachings of the original specification at page 11, lines 1 and 2.

The change to line 37 of Table 1 has been cancelled since this same subject matter is taught in the original specification at page 11, line 28 to page 12, line 1 of the substitute specification. The change to line 37 of Table 1 was not new matter since it only conformed one part of the specification to another part of the orignal specification and also made Table 1 more precise.

The change to line 38 of Table 1 has also been cancelled although the subject matter added at that line was not new matter since it was taught in the original specification at page 12, lines 2-7 (of the substitute specification).

The change at line 39 of Table 1 has been cancelled because the position of the mask 106 is clearly shown in Figures 23A, 23B and 23C to be over the EEPROM device only.

The change at line 40 of Table 1 has been cancelled since the original Figures already make it clear that he N well 62 and P well 66 are the active areas of the NMOS and PMOS devices.

The change at line 41 of Table 1 has been cancelled since the original Figures show at Figures 23A, 23B and 23C that mask 106 protects only the EEPROM device.

The change to line 42 of Table 1 was cancelled because the original Figures 24A, 24B and 24C all show a layer of oxide 112 grown over the second poly everywhere. This same concept is taught in the original specification at page 12, lines 19-20.

The change at line 48 of Table 1 has been cancelled because the original Figures 26A, 26B and 26C all show that the oxide layer has been etched off the horizontal surfaces and left only on the vertical walls of the poly control gates.

The change to line 49 of the table has been cancelled but it is not new matter since it only states the inherent function of the oxide layer 113.

The change to line 51 of Table 1 has been cancelled because this same subject matter is taught at page 13, lines 21-23 of the original specification.

The change at line 53 of Table 1 has been cancelled although the added subject matter which is cancelled here was disclosed in the original part of the specification shown at page 14, lines 2-3 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith.

The changes to lines 54 and 55 of Table 1 have not been cancelled. These changes are not new matter since they merely add to Table 1, subject matter that was originally taught in the main body of the original specification but inadvertently omitted from Table 1.

Specifically, the added subject matter of line 54 of Table 1 is taught in the original part of the specification shown at page 14, lines 4-9 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith. The new boldface addition to line 54 regarding the N+ implant is taught in the original specification as shown at lines 7-9 of page 14 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith. That mask eleven is used to do these two steps is disclosed in the original part of the specification shown at page 14, line 5 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith.

The added subject matter of line 55 of Table 1 is taught in the original part of the specification shown at page 14, lines 10-14 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith. The fact that mask twelve is used to do the P+ boron implant of line 55 is disclosed in the original part of the specification shown at page 14, line 11 of the specification markup having footer VFP-001 Flash subs #2 markup enclosed herewith.

Lines 56 and 57 (misnumbered 54) of Table 1 have been cancelled since they are duplicative of the change to line 54 and are not in the correct sequence taught in the original specification.

Since all changes have been defended on a vigorous line by line basis as not new matter, and since the prior art rejections have been withdrawn, the undersigned believes the application is now in condition for allowance and respectfully requests the Examiner to allow the application.

Respectfully submitted,

Ron Fish

Ronald C. Fish
Reg. No. 28,843
Tel 408 778 3624

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, Va. 22313-1450

On 1/1/04
Date of Deposit

Ron Fish

Ronald Craig Fish, President
Ronald Craig Fish, A Law Corporation
Reg. No. 28,843

CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): Vora		Docket No. V&F-001 CPA1	
Serial No. 08/654,760	Filing Date 5/29/96	Examiner S. Crane	Group Art Unit 2811

Invention:

VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COSTS

OIPE JC25 JAN 0 5 2004 PATENT & TRADEMARK OFFICE

I hereby certify that this **MARKED UP SPECIFICATION**

(Identify type of correspondence)

is being deposited with the United States Postal Service as first class mail in an envelope addressed to: The Commissioner of Patents and Trademarks, MAIL STOP NON FEE AMENDMENT, P.O. BOX 1450, ~~Washington, D.C. 20231-0001~~ ARLINGTON, VA. 22313 on 1/1/04

(Date)

RONALD C. FISH

(Typed or Printed Name of Person Mailing Correspondence)

Ronald C. Fish

(Signature of Person Mailing Correspondence)

Note: Each paper must have its own certificate of mailing.

RECEIVED JAN -7 2004 TECHNOLOGY CENTER 2800

VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

BACKGROUND OF THE INVENTION

The invention pertains generally to the field of semiconductor, nonvolatile memories, and, more particularly, to the field of vertically-integrated, flash EEPROMS which can be manufactured with sufficient density to be cheap enough to compete with rotating magnetic media for bulk memory applications. The vertically-integrated, flash EEPROM according to the teachings of the invention is especially useful in personal computers of the laptop, notebook and palmtop variety although it is broadly applicable to any appliction where large, nonvolatile memory is needed which is physically rugged and competitive with disk drives in price.

Flash EEPROMS are known in the prior art, but the problem to date has been that they cannot be made cheaply enough for them to have mass market appeal. The size of prior art EEPROM cells has been so large, that the number of cells per semiconductor die that can be made with adequate yield was too low to have a cost which was competitive with rotating memories such as disk drives..

Prior art flash EEPROM cells of the most aggressive design made by Intel Corporation of Santa Clara, California are 7-8 square microns using 0.8 micron design rules. With a semiconductor die size of 1 square centimeter, this cell size allows flash EEPROMS of 4-8 megabits to be built for a cost of about $30 per megabit.

In contrast, small disk drives can be manufactured for about $5 per megabyte. Therefore, a need has arisen for a smaller flash EEPROM cell such that more dense memories can be built for lower cost.

SUMMARY OF THE INVENTION

According to the teachings of the invention, a vertically constructed flash EEPROM cell is taught herein which allows a cell size of 2-4 square microns to be achieved. With present 6 inch wafers and 0.8 micron design rules and 40,000-60,000 square mil dies, the cost per megabit of memory cells is a substantial improvement over the $30 per megabit cost of prior art EEPROM cells. With the migration toward 8 inch wafers and 0.6 micron design rules larger die sizes of 100,000-200,000 square mils will be possible, and the cost per megabit of memory cells according to the teachings of the invention should improve greatly.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of a semiconductor substrate at an intermediate stage in construction of a vertical EEPROM cell after the recessed gate window has been formed and first polysilicon has been deposited.

Figure 2 is a cross-sectional view of a semiconductor substrate at an intermediate stage in construction of a vertical EEPROM cell after the floating gate has been formed.

Figure 3 is an equivalent circuit showing the two capacitors of the floating gate structure.

Figure 4 is a vertical cross-sectional diagram of a typical prior art EEPROM cell through the floating gate structure.

Figure 5 is a vertical cross-sectional diagram of the finished vertical EEPROM structure.

Figure 6 is a plan view of a cell array using the vertically oriented EEPROM cells according to the invention.

Figures 7A, B and C through Figures 31A, B and C are cross-sectional views showing various stages of simultaneous construction of an NMOS transistor, a PMOS transistor and a vertically oriented EEPROM cell according to a process compatible with fabrication of CMOS drivers for the EEPROM array according to the teachings of the invention.

Figure 32 is a plan view of four cells in an array of EEPROM cells according to the teachigs of the invention.

Figure 33 is a sectional view through a typical EEPROM cell according to the teachings of the

invention taken along section line A-A' in Figure 32.

Figure 34 is a sectional view through a typical EEPROM cell according to the teachings of the invention taken along section line B-B' in Figure 32.

DETAILED DESCRIPTION OF THE [INVENTION] PREFERRED EMBODIMENT

Referring to Figure 1, there is shown a cross-sectional view of an intermediate stage in the construction of the EEPROM memory cell according to the teachings of the invention. Although a detailed process schedule and series of drawings illustrating the exact method of making one embodiment of the invention will be presented below, Figures 1-3 will be used to summarize the construction of an EEPROM memory cell according to the teachings of the invention.

To reach the stage of construction shown in Figure 1, a one micron deep well is etched into an N type silicon substrate 10 having a resistivity of __________. A P doped region 12 is formed about midway down the well. An N doped region 14 lies above the P type region 12. An oxide layer 16 having a thickness of about 2000 angstroms is grown on top of the substrate. An oxide layer 18 is grown at the bottom of the well and has a thickness of about 1000 angstroms. A thin annular oxide layer, sections of which are shown at 20 and 20', is grown on the sidewalls of the well to insulate a first layer of doped polysilicon 22 which is deposited on the surface of the substrate and into the well.

Figure 2 shows a subsequent stage of construction after an anisotropic etchback to remove the upper portions of the first polysilicon layer and the first polysilicon lying in the bottom of the well above oxide layer 18. This leaves a floating gate comprised of an annular first polysilicon layer, two sections of which are shown at 22 and 22'. This floating gate is isolated from the substrate by the thin oxide layer 20. To complete the electrical isolation of the floating gate layer 22, a layer of ONO insulator 24 is deposited over the surface of the substrate and in the well.

The thickness and integrity of the ONO layer is important to the coupling ratio in an EEPROM which is important in the write process. Referring to Figure 3, there is shown an equivalent circuit of the floating gate and control gate structure shown in Figure 4. Although Figure 4 represents the structure of a typical prior art floating gate EEPROM structure, it is used here to illustrate the functioning of an EEPROM cell and the significance to the write process of the coupling ratio

between the capacitance of capacitor C2 and the capacitor C1 in Figure 3. Capacitor C2 represents the capacitor formed between the control gate 31 and the floating gate 33 in Figure 4. Capacitor C1 represents the capacitor formed between the floating gate 33 and the substrate 39. Layers 35 and 37 are thin oxide or ONO insulating layers (oxide-nitride-oxide) that separate the polysilicon one floating gate layer 33 from the substrate 39, and the polysilicon one floating gate layer from the polysilicon two control gate layer 31, respectively. These two insulation layers separating the conductive polysilicon layers define the capacitors C1 and C2 in Figure 3. Two oxide spacer layers 51 and 53 insulate the self aligned edges of the stacked control gate and floating gate structure.

One problem with the prior art stacked structure of Figure 4 was leakage at the corner 57 where ONO is used for insulation layer 37. At this corner, ONO joins the oxide of the spacer layer 51 (the same holds true for the other side) and the electrical seal against charge leaking out of the floating gate is not perfect because of the concentration of electric field lines at this corner.

The significance of the coupling ratio pertains to the effectiveness of causing injection of electrons or wells into the floating gate 33 so as to alter the trapped charge therein. It is the presence of trapped charge in the floating gate 33 which alters the threshold of the MOS transistor formed by the floating gate 33, and the source region 41 and the drain region 43 in Figure 4. For one state of trapped charge, an inversion of conductivity type in the substrate 39 between the source and drain regions will occur thereby forming a conductive channel through which conduction occurs between the source and drain regions. This channel is symbolized by dashed line 45, and this state of charge can be defined as either a binary 1 or 0. In the other state of charge of the floating gate, no inversion channel occurs, and no conduction between the source and drain occurs. Charge is trapped in the floating gate 33 by tunneling or injection during the write or program process. It is desirable to have the capacitance of capacitor C1 much less than the capacitance of capacitor C2 to insure that sufficient injection or tunnelling of electrons from the source or channel region into the floating gate occurs during the write process. This injection or tunnelling phenomenon occurs when approximatly 15 volts is applied to the control gate terminal 47 in Figure 3 and approximately 8 volts is applied to the source 49 during the write process if C2 is greater than C1. C2 and C1 effectively form a voltage divider between the potential applied to the control gate terminal 47

and the potential of the channel region. It is desirable to have relatively more of the voltage drop from the channel to the control gate terminal 47 occur across capacitor C1 to maximize the tunnelling phenomenon. In other words, when the programming voltage is applied, tunnelling current begins to charge up both capacitors. The smaller capacitor C1 charges up to a higher voltage thereby altering the threshold of the MOS transistor sufficiently to create the inversion channel.

Therefore, since the first oxide layer 35 in Figure 4 or 20 in Figure 2 should be very thin to increase the capacitance of C1 to enhance tunnelling current for writing and erasing, it is necessary for the second oxide layer 37 to be as thin or thinner than the first oxide layer so that C2 is greater than C1. Alternatively, the area of C2 can be made greater than the area of C1. Because of the need for a thin second insulator layer, the material used for the second insulating layer 37 is very important in that it must have high electrical integrity. Generally, ONO is preferred for this purpose because of its high integrity as an electrical insulator and oxide interfaces on both surfaces. Because ONO creates more surface states which would adversely affect the operation of the underlying MOS transistor, ONO cannot be used for the first insulation layer 20 in Figure 2.

ONO layer 24 in Figure 2 is made by oxidizing the underlying layers to a thickness of about 30 angstroms and then depositing approximately 150 angstroms of nitride. Thereafter, steam oxidation of the nitride is performed to form an additional 30 angstroms of oxide. Because of the different dielectric constant of nitride, the overall dielectric constant of the ONO layer 24 is approximately the same as that of 100 angstroms of oxide. ONO works especially well to preserve the trapped charge in the floating gate to alleviate a problem of escaping charge at the corners of the floating gate which existed in the prior art.

After the ONO layer 24 is deposited, a second layer of doped polysilicon 28 is deposited to fill the well and is etched to form the word line.

Figure 5 shows in vertical section the completed device. To reach the state of construction shown in Figure 5, a layer of oxide 29 is grown on the second polysilicon layer 28. Then a mask is formed over the second polysilicon layer 28 to protect the portion thereof overlying the well which it fills. Thereafter, an anisotropic etch is performed to etch down through the polysilicon layer 28, the ONO layer 24, the oxide layer 16 and part of the way through the N-type silicon layer 14 to open a

contact well for the bit line 30.

After this contact well is opened, an annular oxide spacer, sections of which are shown at 32 and 32', is formed to seal and insulate the sides of the structure from the bit line to be formed next. The oxide spacer is formed by growing or depositing a layer of oxide over the entire structure and anisotropically etching it back to leave the vertical sections of oxide.

The bit line is shared by all devices in a row and is formed by depositing a third layer of polysilicon 30 over the entire structure and etching it to selectively make contact with the N-type silicon layer 14 which forms the drain of the vertical annulus MOS transistor formed inside the well. The source of the vertical MOS transistor is the N-type substrate 10. The channel region for this transistor is formed by the P-type silicon layer 12. The gate oxide between the channel region and the floating gate 22 is oxide layer 20. The control gate is comprised of second polysilicon layer 28, and extends down into the page and up out of the page to form the word line.

Figure 6 shows a plan view of the EEPROM cell. Field oxide 40 defines the outer boundaries of the N-type silicon layer 14 through which the wells [14] 13 and 42 are formed. The polysilicon or metal bit line 30 (polysilicon is shown and preferred for better step coverage) runs from left to right over and in contact with the N-type silicon layer 14 and slightly overlaps the field oxide layer. The bit line also overlaps the word line polysilicon 28 which fills the well 11. The details of the structure down inside the well are not shown in Figure 6 for simplicity.

The length of the cell shown in Figure 6 is equal to the dimension A defining the length of the well plus the dimension B which defines the pitch or minimum spacing between the wells. In Figure 6, the next row of wells is represented by wells 48 and 50. For 0.6 micron design rules, A = 0.6 micron and B = 0.6 microns for a total length of 1.2 microns.

The width of the cell is equal to the dimension C which defines the width of the well, plus the dimension D which defines the overlap of the second polysilicon layer 28 past the edge of the well, plus the dimension E equal to the pitch between the second polysilicon word lines 28 between columns. For 0.6 micron design rules, C = 0.6 microns, D = 0.05 microns and E = 0.6 microns for a total cell width of 1.3 microns. Thus, the total cell area for 0.6 micron design rules is 1.56 square microns.

With a cell size of 1.56 square microns, a 64 megabit EEPROM memory can be built on a die of 1-2 square centimeter size. With 6 inch wafers, the wafer area is 28 square inches. At 6.54 square centimeters per square inch, a 6 inch wafer contains 182 square centimeters. With a die size of 2 square centimeters, a 6 inch wafer yields about 90 die. Because well known redundancy techniques can be used to repair defective cells, yields in EEPROM production are typically high, averaging around 80 percent. Thus, a typical production run will yield about 72 good die. Typical production costs for a 6 inch wafer are about $500, so the cost per 64 megabit (8 megabytes) die is about $6.94 or about $0.86 per megabyte. A 40 megabyte EEPROM memory using the teachings of the invention would cost about $34.72. This cost should come down with the introduction of 8 inch wafers at 0.6 micron line widths. Typical costs are expected to be about $3.87 per 8 megabyte EEPROM memory or 48 cents per megabyte for a total cost for a 40 megabyte memory of $19.37. Of course any change in any of the numbers of assumptions or numbers used in the above calculations will yield different costs per megabyte. Todays cost for typical prior art EEPROM memory sold by Intel Corporation is about $30 per megabyte manufactured using 0.8 micron design rules. Note that in the above cost calculations, 0.6 micron linewidths were assumed. Costs for prior art EEPROM cells using 0.6 micron design rules should fall to about $15 per megabyte.

A detailed description of how to make the EEPROM memory cell according to the teachings of the invention follows in connection with the discussion of Figures 7A, B and C through Figures 30A, B and C. The preferred process is compatible with CMOS processing so that the EEPROM memory can be built on the same die with CMOS drivers. Accordingly, in each of Figures 7A, B and C through Figures 30A, B and C, the figures in the left column labelled Figure _A is the corresponding NMOS structure and the figures in the right column labelled Figure _C is the corresponding PMOS structure. A summary of the process is given in Appendix A. In Appendix A, the individual steps in the process are numbered, and the steps in which the masks are used are given in the column second from the right. The figure numbers in the rightmost column of Appendix A show the state of construction after the steps preceding the line on which the particular figure number is listed have been completed.

Referring to Figures 7A, B and C, there is shown the state of construction after the first [12]

nine steps in Appendix A. To reach the state of construction shown in Figures 7A, B and C, a P-type silicon substrate having a conventional resistivity is used as the starting material.

Then a layer of oxide (silicon dioxide) is thermally grown to a thickness of approximately 300 angstroms.

Next a layer of nitride (silicon nitride) is deposited to a thickness of about 1000 angstroms using chemical vapor deposition (CVD), low pressure CVD (LPCVD) or plasma enhanced chemical vapor deposition (PECVD).

A layer of photoresist is then deposited and developed using the first level twin-well mask to define the twin wells needed to form CMOS devices.

After forming the twin well mask layer of photoresist, the nitride layer is etched away over an area to be implanted with phosphorous to form [an] the N-type wells 62 and 64 in which to form the PMOS device and the EEPROM device. Any process for etching the nitride will suffice.

To form the N-well, phosphorous is implanted to a depth of about 3000 angstroms using conventional dosage levels. Then the phoshorous is driven in and the N-well area has another layer of oxide grown thereover using a 1000 degree centigrade oven for one hour. This leaves the structure as shown in [Figure 1] Figures 7B and 7C with an N-well 62 for the PMOS device, and N-well 64 in which the EEPROM device is to be constructed[, and a P-well 66 in which the NMOS device is to be built].

Next, the photoresist and nitride are stripped, and boron is implanted to form the P-well 66. Both wells are then driven deeper using a 1100 degree centigrade oven for 5 hours to form wells that [art] are 5-6 microns deep.

The oxide is then etched away over the N-wells 62 and 64 to clear the substrate surface for further processing.

Finally, a ~~300 angstrom thick oxide layer is grown and a~~ 1000 angstrom ~~thick~~ nitride layer is [grown] formed as shown in Figures 8A, B and C with the oxide and nitride layers shown as a single layer at 68.

Next, a layer of photoresist is deposited and an active mask (mask 2) is used to cross-link (develop) sections thereof to leave the structure as shown at Figures 8A, B and C with a photoresist

section 70 over the P-well, photoresist section 72 over the EEPROM cell area and photoresist section 74 over the N-well.

The oxide/nitride layer 68 is then etched using the photoresist as a mask to leave the structure as shown in Figures 9A, B and C.

A field implant must be performed to implant boron at the edges of the active area of the NMOS device to prevent the formation of parasitic channels, i.e., unintended MOS transistors. To perform this implant, it is necessary to mask off the N well of the PMOS device. This is done by depositing a layer of photoresist 76 and developing it with the field implant mask, i.e., mask 3 to leave the second photoresist layer 76 covering the N well 62. A boron implant is then performed to deposit the P-type field implant impurities shown at 78 in Figure 10A.

After the field implant, the field regions outside the active areas are oxidized to a thickness of 6000 angstroms to leave the structure as shown in Figures 11A, B and C. The field oxide is shown at 80. The areas under the field oxide remain doped so they do not invert and form parasitic MOS devices.

Next the fourth mask is used to remove the nitride portion of layer 68 of oxide/nitride by protecting all structures with photoresist except the oxide/nitride layers 68 over the EEPROM cells. After developing the photoresist with the fourth mask, a conventional oxide/nitride etch is performed to leave the structure as shown in Figures 12A, B and C with photoresist layer 69 protecting the NMOS and PMOS active areas. This leaves a thin layer of pad oxide (not shown) over the EEPROM active areas.

Leaving the photoresist 69 over the NMOS and PMOS wells to protect them, a boron ion implantion is performed through the pad oxide (not shown) to form the buried P region 82 below the surface of the N well in which the EEPROM cell is to be formed. Typically, the dosage for this implant will be 1E+12 (on the order of 10 to the 12th power) with an energy level of 100 KEV. This implant forms the channel region in the vertical annular EEPROM cell. As the term annular is used herein, the horizontal cross section through the EEPROM transistor below the surface of the substrate can be either circular, square, rectangular or some other shape.

Next, leaving the photoresist in place over the NMOS and PMOS devices, an arsenic implant

is performed at a lower energy level to redope the area 86 below the surface of the substrate but above the P region 82 back to N type to act as the drain region of the vertical MOS transistor EEPROM device, as shown in Figures 13A, B and C. Typically, 30 KEV is used with a dose of 1E+14.

Still leaving the photoresist in place over the NMOS and PMOS devices, a layer of oxide 84 is grown over the EEPROM cell to leave the structure as shown in Figures 14A, B and C.

The EEPROM cell area will be used to form two vertical EEPROM devices. To start this process, a layer of photoresist (not shown) is deposited and a fifth mask is used to develop the photoresist so as to open two cell etch windows over the EEPROM cell area. An anisotropic plasma etch process is then used to etch ~~vertically down~~ through the oxide layer [86] 84 and etch ~~vertically~~ down into the silicon to form two wells 88 and 90 also called recessed gate windows. These recessed gate windows must have sufficient depth to penetrate the N layer 86 and the P layer 82 and extend into the N well 64 of the EEPROM cell. This leaves the structure as shown in Figures 15A, B and C.

A pad oxide layer (not shown) 300 angstroms thick is grown next. This layer covers the first nitride layer 68 over the NMOS and PMOS devices, the oxide layer 84 over the EEPROM cells and covers the walls and bottoms of the [recessed gate windows] ~~wells~~ 88 and 90. This pad oxide layer protects the underlying structures from a second layer of nitride to be deposited next.

A second layer of nitride 92 approximately 500 angstroms thick is then deposited over the entire structure. This layer covers the walls and the bottom of the two [recessed gate windows] ~~wells~~ 88 and 90 and covers the ~~entire horizontal~~ top surface of the substrate ~~extending laterally in all directions~~.

An anisotropic etchback is then performed to remove all portions of nitride layer 92 on horizontal surfaces and leave only [except] those portions on vertical surfaces, i.e., all nitride of layer 92 is removed except those portions on the vertical walls of the recessed gate windows to leave the structure as shown in Figures 17A, B and C.

Next, a layer of oxide insulator 96 is grown on the bottoms of the **recessed gate windows.** ~~wells 88 and 90, but the nitride on the vertical walls of the wells prevents the oxide 96 from growing~~

~~on the vertical walls of the wells 88 and 90.~~ The nitride of layer 92 is then removed from the walls of the [recessed gate windows] ~~wells~~ 88 and 90 using a wet etch to leave the structure as shown in Figures 19A, B and C.

The pad oxide (not shown) underneath the second nitride layer 92 is then removed ~~from the vertical walls of the wells 88 and 90~~ in a wet etch. Because the pad oxide layer was not separately shown, the structure after its removal looks as shown in Figures 19A, B and C.

A thin gate oxide layer 100 is then grown on ~~exposed silicon surfaces including the vertical~~ the walls of the **recessed gate windows** ~~wells~~ 88 and 90 to insulate the polysilicon floating gate to be formed later from the [silicon] ~~doped substrate~~ layers 86 (drain), 82 (channel) and 64 (source). Typically, this gate oxide is grown to a thickness of 90 to 100 angstroms in a process conventional to MOS devices.

Next, a layer of P type doped polysilicon 102 is deposited over the complete structure from which the floating gate 22 in Figure 5 will be formed to leave the structure as shown in Figures 20A, B and C. Typically, about 1000 angstroms of polysilicon is deposited and is doped P type with chemical dope of phosphorous either during or after deposition to a resistivity of 50 ohms per square.

To form the floating gate, the doped polysilicon is etched back off all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure shown in Figure 5 and are self aligned with the walls of the **recessed gate windows** ~~wells~~ 88 and 90 **because no horizontal component of doped polysilicon is left on the surface of the substrate or on the bottom of the recessed gate windows which means no portion of the doped polysilicon will ever extend beyond the perimeter of the recessed gate window (see Figure 21B for the configuration of the doped polysilicon floating gate 102 after the etchback). No mask is used for the etchback of the doped polysilicon layer 102 as can be seen from study of Table 1 steps 33 and 34 where no mask is recited as being used during the etchback. All steps that use masks are recited in Table 1 as using a mask and the mask number is given in the third column from the left.** ~~without using a mask because of the fact that the etchback removes all portions of polysilicon 102 on horizontal surfaces on top of the substrate~~

~~and at the bottoms of the wells 88 and 90~~.

Electrical isolation of the floating gate is accomplished by formation of another oxide-nitride-oxide layer 104 over the entire wafer to leave the structure as shown in Figures 22A, B, C. Typically, the ONO layer 104 is formed to a thickness of 150 angstroms by a conventional process.

At this point in the process, construction of the NMOS and PMOS devices is started in parallel with the completion of the EEPROM devices. The first step in this process is to deposit a layer of photoresist and develop it with mask 6 to form an ONO protect mask 106 over the EEPROM cell area as shown in Figure 23B. Then an ONO etch and a nitride etch are performed to remove the ONO layer 104 and the nitride layer 68 over the NMOS and PMOS transistor active areas to leave the structure as shown in Figures 23A, B and C. The pad oxide (not shown) under the nitride layer 68 is left in place to protect the silicon from the threshold adjust implant to be performed next.

A threshold voltage adjustment is next performed by a conventional boron implant to implant charges into the surface region of the N well 62 and the P well 66 to adjust the voltages at which the PMOS and NMOS devices turn on. The design is such that one CMOS device threshold voltage is too low and the other CMOS device threshold voltage is too high before the threshold adjust implant. Then the threshold voltages are adjusted simultaneously in the proper directions by the threshold adjust implant.

After the implant, the pad oxide (not separately shown) that was under the oxide layer 68 is etched away to prepare the NMOS and PMOS devices for growth of a thin gate oxide. During this process the photoresist mask 106 is left in place to protect the EEPROM cell area.

A thin gate oxide layer 108 is then grown over the N well 62 and the P well 66 ~~of the NMOS and PMOS devices~~ to electrically insulate a gate electrode to be formed later from the underlying silicon. During this process the photoresist mask 106 is left in place to protect the EEPROM cell area.

Next, the photoresist mask 106 is removed ~~over the EEPROM device~~, and a second doped polysilicon layer 110 is [then] deposited to a thickness of about 3000 angstroms. The control gates for the PMOS, NMOS and EEPROM devices will be formed from this polysilicon layer 110. This second polysilicon layer also fills the recessed gate windows 88 and 90 and covers the ONO layer 104.

A thin layer of silicon dioxide 112 is then grown over the entire second polysilicon layer 110 to a depth of about 2000 angstroms.

A seventh mask is then used to develop a layer of photoresist deposited over the second polysilicon layer 110 and oxide 112 for purposes of etching the second polysilicon layer to form the control gates of the PMOS and NMOS devices and of the EEPROM cells and the word lines corresponding to word line 28 in Figures 5 and 6. After the etch of the second polysilicon by a conventional process, the structure looks as shown in Figures 25A, B and C except that an LDD phosphorous implant to form the source and drain regions of the NMOS device has not yet been performed.

To form the source and drain regions of the NMOS devices, an 8th mask is used to develop a layer of photoresist to form an LDD implant mask over the PMOS and EEPROM devices. Then phosphorous is implanted in a conventional process using the etched second polysilicon layer 110 over the NMOS device as a mask to form self aligned LDD regions (lightly doped drain regions) shown at 114 in Figure 25A. Later, more heavily doped, deep source and drain regions will be formed, but the LDD implants prevent short channel problems.

To protect the sidewalls of the control gates of the NMOS, PMOS and EEPROM devices, a spacer oxide deposition is performed to a depth of 3000 angstroms and then the spacer oxide is etched back to form the spacer oxide regions 114 on the ~~vertical~~ sidewalls of the polysilicon control gates formed from second polysilicon layer 110. The spacer etch is an anisotropic etch to remove the spacer oxide from only the horizontal surfaces.

Referring to Figures 27A, B and C, to open contact holes 118 and 120 to the EEPROM cell, a layer of photoresist is deposited and developed with a ninth mask to form a cell contact etch mask layer 116 protecting the PMOS and NMOS devices. The developed photoresist of layer 116 is also located so as to bound the outer limits of the contact holes to be etched through the ONO layer 104 and the oxide layer 84. The other boundaries of these contact holes are self aligned with the outer edges of the spacer oxide 114. Oxide layers 113 are then formed on top of the second polysilicon control gates 110 using the photoresist 116 as a mask as shown in Figure 28B.

The ONO etch and oxide etch is then performed to leave the structure as shown in Figures

27A, B and C with contact holes 118 and 120 to the N type ~~drain~~ layer 86 for the bit line connections (not shown).

To form the bit lines corresponding to the bit line 30 in Figures 5 and 6, a layer of metal or polysilicon 122 is deposited over the structure. Metal is shown at 122 in Figure 28B, but doped polysilicon is preferred for better step coverage.

Photoresist is then deposited and a tenth mask is used to develop it to form a protective layer over the EEPROM devices so as to allow removal of the metal or polysilicon off the NMOS and PMOS devices and so as to define the outlines of the bit lines. The metal or polysilicon 122 is then etched into the shape of the bit lines and removed from over the PMOS and NMOS devices to leave the structure as shown in Figures 28A, B and C.

Next, to complete the NMOS device, an N+ arsenic implant must be performed in the P well. To accomplish this, a layer of photoresist is deposited and developed with an eleventh mask to protect the EEPROM cell and the PMOS active area by photoresist which is not shown in the figures. An N+ arsenic implant is then performed using this photoresist exposing the P well and the polysilicon 110 and the spacer oxide 114 as a mask to form the self-aligned source and drain regions 130 and 132.

To complete the PMOS device, another layer of photoresist is deposited and developed with mask 12 to expose the N well 62 and protect the EEPROM active area and the P well 66 ~~of the NMOS device~~. A P+ boron implant is then performed using this photoresist as a mask and the second polysilicon control gate 110 and spacer oxide 114 as a mask to form self-aligned source and drain regions 134 and 136. ~~Next, the photoresist is removed and a new layer of photoresist is deposited and developed using mask 12 to protect the EEPROM device and the N well 62 of the PMOS device area and expose the P well 66 of the NMOS device. An N+ arsenic implant is performed using this layer of photoresist and the control gate 110 and oxide spacer layers 114 of the NMOS device as implant masks to form self aligned source and drain layers 130 and 132 for the NMOS device.~~ This leaves the structure as shown in Figures 29A, B and C.

To repair the implant damage, the structure is annealed at 1000 centigrade for 30 seconds.

To passivate the structure, a BPSG deposition is performed to a thickness of 6000

angstroms.

To complete the NMOS and PMOS devices, contacts to the source and drains of the PMOS and NMOS devices must be made. To do this, a layer of photoresist is deposited and developed using contact mask 13. An etch is then performed to cut the contact holes 138, 140, 142 and 144 through the BPSG layer 146.

After a contact reflow to soften the edges for better step coverage , a layer of metal is then deposited to 7000 angstroms and etched to form the contacts 148, 150, 152 and 154 to complete ~~the structure as shown in Figures 31A, B and C.~~

Referring to Figure 32, there is shown a plan view of four cells in an array of vertically oriented EEPROM cells according to the teachings of the invention and constructed according to a process which is compatible with the simultaneous formation of CMOS devices on the same die. The outlines of two recessed gate windows in which two EEPROM cells are formed are shown at 88 and 90. First polysilicon word lines are shown at 110. The metal or second polysilicon bit lines are shown at 122. The drain regions of the EEPROM cells are shown at 123 and 125.

Figure 33 is a cross-sectional view taken along section line A-A' in Figure 32 of the lower two EEPROM cells having recessed gate windows shown at 127 and 129 in Figure 32. Figure 34 is a cross-sectional view of the EEPROM cells in recessed gate windows 90 and 129 in Figure 32 taken along section line B-B' therein. Structural elements in Figures 33 and 34 corresponding to elements in Figures 7A, B and C through 31A, B and C and Figure 32 have the same reference numerals.

There is given below a table summarizing the above described process of building the flash EEPROM according to the teachings of the invention which is compatible with simultaneous fabrication of CMOS devices on the same die.

APPENDIX A

PROCESS FLOW FOR CONSTRUCTING A SELF-ALIGNED EEPROM MEMORY CELL COMPATIBLE WITH CMOS DRIVERS ON THE SAME DIE

STEP	DETAILS	MASK	FIGURE
1. Start with silicon substrate	P-Type, Resistivity _		
2. Grow a layer of oxide	Approx. 300 angstroms		

3. Deposit a layer of nitride	Approx. 1000 angstroms		
4. Deposit and develop a layer of photoresist using twin well mask		Mask 1	
5. Etch nitride layer over portion of substrate to become N-wells 62 and 64			
6. Form N-wells 62 and 64 with phosphorous implant	3000 anstroms deep, conventional dosage		
7. Drive phosphorous and re-oxidize N-wells 62 and 64	1000 degrees C, 1 hour		
8. Strip photoresist and nitride			
9. Implant Boron to form P-well 66			
10. Drive the N and P wells 62, 64 and 66 deeper	1100 degrees C, 5 hours, 5-6 microns deep after drive		Figure7 A, B and C
11. Etch oxide over N-wells 62 and 64 to clear the surface thereof for further processing			
12. Grow pad oxide	300 angstroms		
13. Deposit nitride layer	1000 angstroms		
14. Deposit photoresist and use active mask to develop photoresist to define etch masks 70, 72, 74 for active areas		Mask 2	Figure 8A, B and C
15. Etch oxide/nitride layer 68 to define active areas			Figure 9A, B and C
16. Deposit a layer of photoresist and develop using a field implant mask to form field implant mask 76		Mask 3	Figure 10A, B and C
17. Boron implant to deposit field implant impurities in P well.	Conventional dosage and energy		
18. Grow field oxide	6000 angstroms		Figure 11A, B and C

19. Deposit photoresist and develop with mask 4 to leave exposed only the ONO layer 68 over the EEPROM cells		Mask 4	
20. Etch away nitride portion of oxidie/nitride [ONO] layer 68 over EEPROM cell to leave pad oxide			Figure 12A, B and C
21. Implant boron ~~through the pad oxide~~ to form P region 82 below substrate surface throughout N well in which EEPROM is to be formed to make channel region 12 of finished device as shown in Figure 5.	100 KEV, 1E+12		
22. Implant arsenic to redope to N type region 86 below surface but above P layer 82 ~~to act as a drain of the vertical MOS EEPROM device~~	30 KEV, 1E+14		Figure 13A, B and C
23. Grow layer of oxide 84 over EEPROM cell area	2000 angstroms		Figure 14A, B and C
24. Deposit layer of photoresist and use cell etch mask 5 to develop to open windows for etching [recessed gate windows] wells 88 and 90		Mask 5	
25. Anisotropically etch [recessed gate windows] ~~wells~~ 88 and 90 through ~~oxide layer 84 and~~ N layer 86 and P layer 82 into N well 64			Figure 15A, B and C
26. Grow pad oxide layer over whole substrate ~~including vertical walls of wells 88 and 90~~ to protect underlying structures from second nitride layer	300 angstroms		
27. Deposit second nitride layer 92 which is thinner than first nitride layer 68	500 angstroms		Figure 16A, B and C
28. Perform anisotropic nitride etchback to remove nitride of layer 92 on all horizontal surfaces and leave it covering only the vertical walls of the [recessed gate windows] ~~wells~~ 88 and 90	anisotropic etch		Figure 17A, B and C

29. Grow oxide 96 on bottoms of ~~[~~recessed gate windows~~] wells~~	2000 angstroms		Figure 18A, B and C
30. Cell nitride strip using a wet etch to remove nitride layer 92 from ~~vertical~~ walls of recessed gate windows ~~wells~~ 88 and 90.	dip off nitride in wet etch		Figure 19A, B and C
31. Pad oxide strip ~~to remove pad oxide (not shown) from vertical walls of wells 88 and 90.~~	dip off pad oxide in wet etch		
32. Grow thin gate oxide layer 100 ~~on at least the vertical walls of the wells 88 and 90 to insulate the floating gate to be formed later from the drain, channel and source regions at the intersection of the walls of the wells 88 and 90 with these regions of the substrate the wells penetrate.~~	90-100 angstroms, conventional process		
33. Deposit doped polysilicon layer 102 from which floating gate is to be formed	1000 angstroms doped P type to 50 ohms per square		Figure 20A, B and C
34. Etch back doped polysilicon layer 102 from horizontal surfaces to leave floating gates ~~only on vertical surfaces of walls of wells 88 and 90 thereby forming floating gates which are self aligned with the walls of the wells 88 and 90.~~			Figure 21A, B and C
35. Form Oxide-Nitride-Oxide layer 104 above floating gates	Conventional process, 150 angstroms		Figure 22A, B and C
36. Form ONO protect mask 106		Mask 6	
37. ONO etch, nitride etch to clear PMOS and NMOS active areas for transistor formation. ~~Pad oxide layer under nitride is left in place over PMOS and NMOS devices to protect surface of silicon from threshold adjust implant.~~			Figure 23A, B and C
38. Threshold voltage adjust implant ~~to adjust thresholds of PMOS and NMOS devices to proper levels simultaneously.~~	Boron		

39. Leaving photoresist mask 106 in place ~~to protect EEPROM device~~, etch away pad oxide under first nitride layer 68 to expose N well and P well silicon			
40. Leaving photoresist mask 106 in place, grow thin gate oxide 108 over N well 62 and P well 66 ~~of NMOS and PMOS devices.~~	150 angstroms		
41. Remove photoresist mask 106 ~~over the EEPROM device~~, and deposit a doped second polysilicon layer 110 over entire structure	3000 angstroms		
42. Oxidize second polysilicon ~~to grow a layer of oxide insulator over the entire second polysilicon layer~~	2000 angstroms		Figure 24A, B and C
43. Deposit photoresist, and use 7th mask to develop a second poly etch mask		Mask 7	
44. Etch second polysilicon 110 and overlying oxide to form control gates and word lines corresponding to word line 28 in finished device of Figure 5			
45. Deposit photoresist and develop using 8th mask to protect PMOS and EEPROM devices to form LDD implant mask		Mask 8	
46. Phosphorous LDD implant using control gate poly as a mask to form self-aligned LDD source and drain regions of NMOS devices.	Conventional process		Figure 25A, B and C
47. Deposit spacer oxide	3000 angstroms		
48. Anisotropically etch spacer oxide ~~from horizontal surfaces~~ to leave spacers on ~~vertical~~ sidewalls of polysilicon control gates.			Figure 26A, B and C
49. Deposit photoresist and develop with Mask 9 to protect the NMOS and PMOS devices for a bit line contact hole etch and reoxidize tops of second polysilicon 110 to form oxide layer 113 ~~to insulate top of control gate from bit line to be formed later.~~		Mask 9	Figure 27A, B and C

50. Etch self aligned bit line contact holes 118 and 120 through ONO 104 and oxide 84			
51. Deposit bit line metal or ~~doped~~ poly~~silicon~~ 122	5000 angstroms		
52. Deposit layer of photoresist and develop using 10th mask to form protective mask layer over NMOS and PMOS devices		Mask 10	
53. Etch bit line metal layer 122 to form bit lines ~~and remove metal or polysilicon 122 from PMOS and NMOS devices~~			
54. Deposit photoresist and develop using mask 11 to expose N well 62 and protect EEPROM active area 64 and P well 66 of NMOS device. An N+ arsenic implant is then performed using this photoresist exposing the P well and the polysilicon 110 and the spacer oxide 114 as a mask to form self-aligned source and drain regions 130 and 132.		Mask 11	
55. A P+ boron implant is then performed to form self aligned source and drain regions 134 and 136 of PMOS device.		Mask 12	
~~[53.] 56. Deposit photoresist and develop using mask [11] 12 to expose P well 66 and protect EEPROM active area 64 and N well 62~~		~~Mask [11] 12~~	
~~54. N+ arsenic source and drain implant for NMOS device~~	Arsenic, conventional process	~~[Mask 12]~~	Figure 29A, B and C
55. Anneal implants	1000 C, 30 sec		
56. BPSG passivation deposition	6000 angstroms		
57. Deposit photoresist and develop with contact mask 13 to form mask for contact holes for NMOS and PMOS devices		Mask 13	
58. Etch contact holes			
59. Contact reflow		Mask 14	

60. Metal deposition, mask and etch to form contacts 148, 150, 152 and 154	7000 angstroms	Mask 15	Figure 31A, B and C

Although the invention has been disclosed in terms of the preferred and alternative embodiments described herein, those skilled in the art will appreciate different variations and alternatives which may be used to embody the teachings of the invention. All such variations and alternatives are intended to be included within the scope of the claims appended hereto.

What is claimed:

1. A nonvolatile memory cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by alternating N-type and P-type doped layers in said substrate intersecting a well etched into said substrate, said well having a floating gate of conductive material formed therein and insulated from and overlying said alternating N-type and P-type materials by a layer of gate insulating material;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said flaotign gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate.

2. A nonvolatile memory cell, comprising:

a semiconductor substrate of a first conductivity type having a surface;

a buried layer in said semiconductor substrate doped so as to have a second conductivity type suitable to act as a channel region of a vertical MOS transistor formed in said substrate;

a first region of said semiconductor substrate between said buried layer and said surface of said substrate, and a second region of said semiconductor substrate below said buried layer, both said first and second regions being doped so as to have a first conductivity type;

a first layer of insulating material covering said surface of said substrate;

a recessed gate window in the form of a well etched in said semiconductor substrate through said first layer of insulating material, said well being deep enough to penetrate said buried layer such that the side walls of said recessed gate window intersect said buried layer and said first and second regions of said semiconductor substrate;

a second insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a floating gate comprising a conductive material formed on said gate insulating layer with an insulating layer formed over said conductive material so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said intersection of said well with said buried layer;

a word line comprising conductive material deposited on said first insulating layer so as to extend into said well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed over said word line; and

a bit line formed over said surface of said semiconductor substrate but insulated from

said word line by said second layer of insulating material, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transistor.

ABSTRACT OF THE DISCLOSURE

A nonvolative memory in the form of a flash EEPROM with high density and low cost. A vertical MOS transistor is formed in well etched into a semiconductor substrate, the substrate having a buried layer of doped material of a first conductivity type acting as the channel region. Source and drain regions of this transistor comprise second conductivity type layers doped in the substrate above and below the buried layer. A thin gate oxide or oxide-nitride-oxide (ONO) layer is formed in the well and a floating gate of polysilicon is formed over the gate oxide. A layer of oxide or ONO is formed over the floating gate, and a second polysilicon or metal layer is used to fill the well to form the control gate and word line. A bit line is formed of a layer of metal or polysilicon deposited over an insulating layer on top of the word line and makes contact with the drain of the vertical MOS transistor through a contact window formed adjacent the well.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed:Commissioner of Patents and Trademarks, Washington D.C. 20231 on

(Date Of Deposit)_____________________________

Express Mail Receipt Number:____________________________________

____

Ronald Craig Fish, President
Ronald Craig Fish a Law Corporation
Reg. No. 28,843